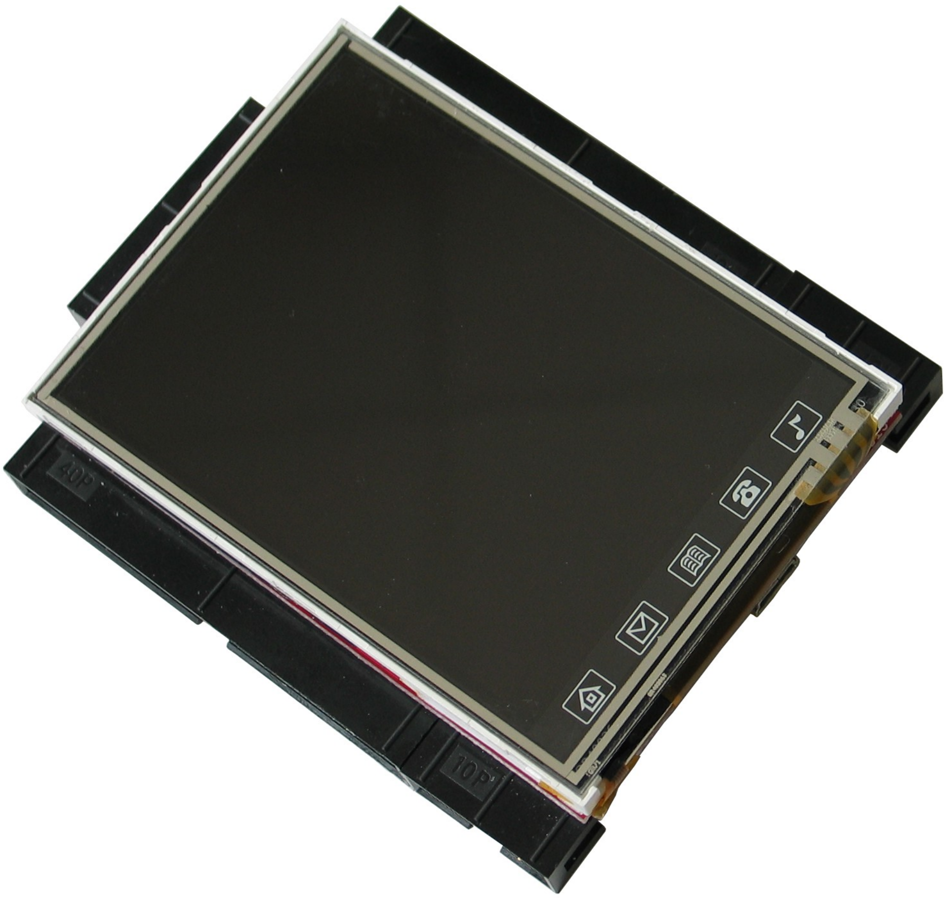


STM32-LCD development board

User's manual

All boards produced by Olimex are ROHS compliant

Revision C, May 2014

INTRODUCTION:

STM32-LCD is development prototype board with STM32F103ZE microcontroller from STMicroelectronics. This powerful microcontroller supports various serial interfaces such as USB, USART, SPI. In addition you will find also accelerometer, JTAG, TFT LCD, mini SD/MMC card connector on this board and most of the GPIOs are on extension headers where you can connect your additional circuits. All this allows you to build a diversity of powerful applications to be used in a wide range of situations.

BOARD FEATURES:

- Microcontroller – STM32F103ZE – high-performance ARM® Cortex™-M3 32-bit RISC core operating at a 72 MHz frequency, high-speed embedded memories (Flash memory – 512 Kbytes and SRAM – 64 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses.
- JTAG connector
- EXT connector
- UEXT40 connector
- UEXT1 connector
- UEXT2 connector
- EXT_PWR connector
- Mini SD/MMC
- Mini USB
- LCD TFT 320x240 pixels colored with touch screen
- Power source connector
- Accelerometer
- 8 MHz crystal oscillator
- Reset circuit
- Clock circuit
- PCB: FR-4, 1.5 mm (0,062"), soldermask, silkscreen component print
- Dimensions 79.2x57.6 mm (3.12x2.27)”

ELECTROSTATIC WARNING:

The **STM32-LCD** board is shipped in protective anti-static packaging. The board must not be subject to high electrostatic potentials. General practice for working with static sensitive devices should be applied when working with this board.

BOARD USE REQUIREMENTS:

Cables: The required cables depend on the programmer/debugger that you use. Additionally, you might need USB mini cable for USB connection

Hardware: You need a JTAG or SWD debugger or programmer to be able to program the board. The board has a standard 20-pin JTAG connector and typical layout (further detailed later in the document).

You may check on our products ARM-JTAG-COOCOX, ARM-USB-OCD-H, ARM-USB-TINY-H.

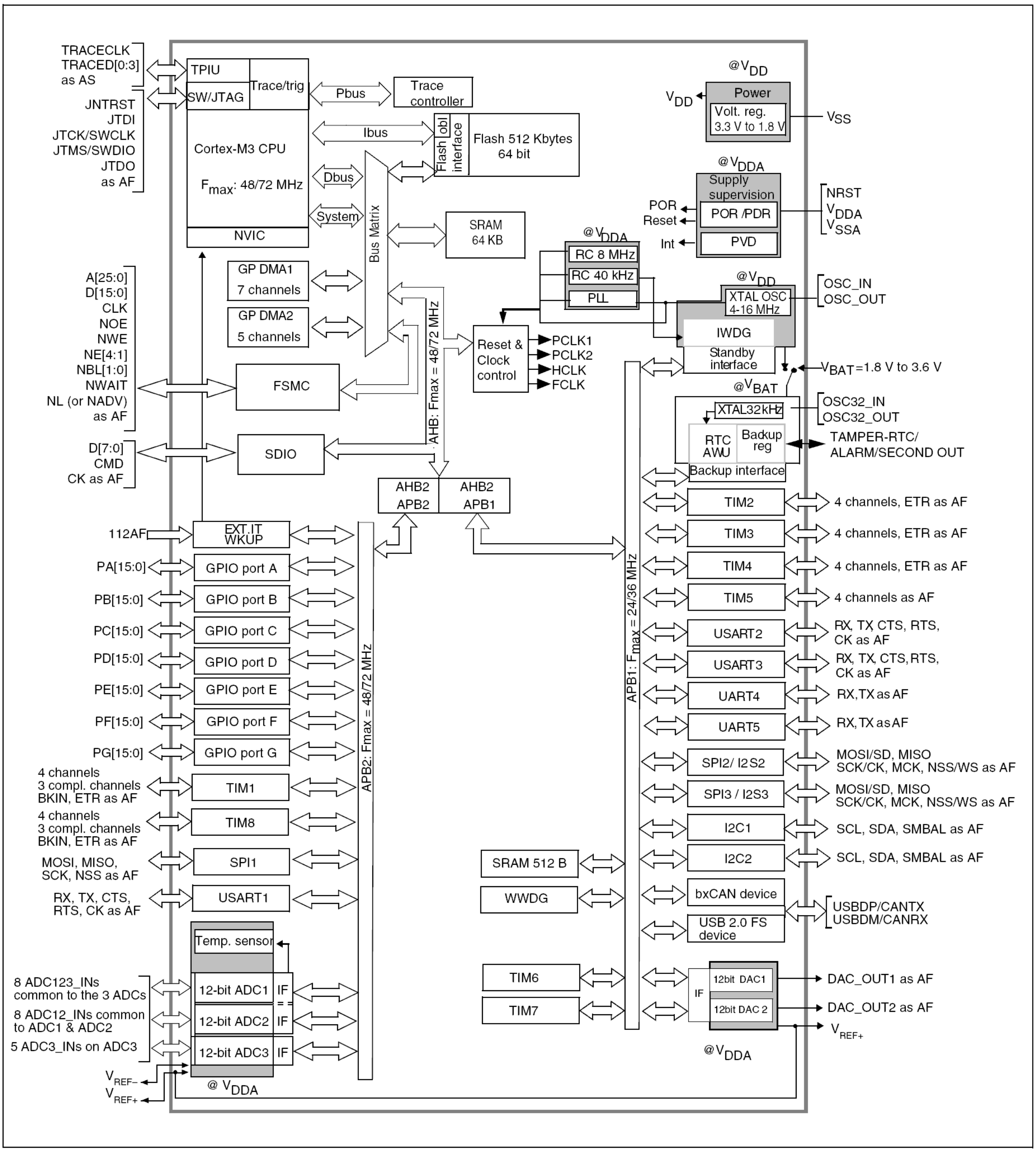
PROCESSOR FEATURES:

STM32-LCD use High-density performance line ARM-based 32-bit MCU with these features:

- Core: ARM 32-bit Cortex™-M3 CPU
  - 72 MHz maximum frequency, 1.25 DMIPS/MHz (Dhrystone 2.1) performance at 0 wait state memory access
  - Single-cycle multiplication and hardware division
- Memories
  - 512 Kbytes of Flash memory
  - 64 Kbytes of SRAM
  - Flexible static memory controller with 4 Chip Select. Supports Compact Flash, SRAM, PSRAM, NOR and NAND memories
  - LCD parallel interface, 8080/6800 modes
- Clock, reset and supply management
  - 2.0 to 3.6 V application supply and I/Os
  - POR, PDR, and programmable voltage detector (PVD)
  - 4-to-16 MHz crystal oscillator
  - Internal 8 MHz factory-trimmed RC
  - Internal 40 kHz RC with calibration
  - 32 kHz oscillator for RTC with calibration
- Low power

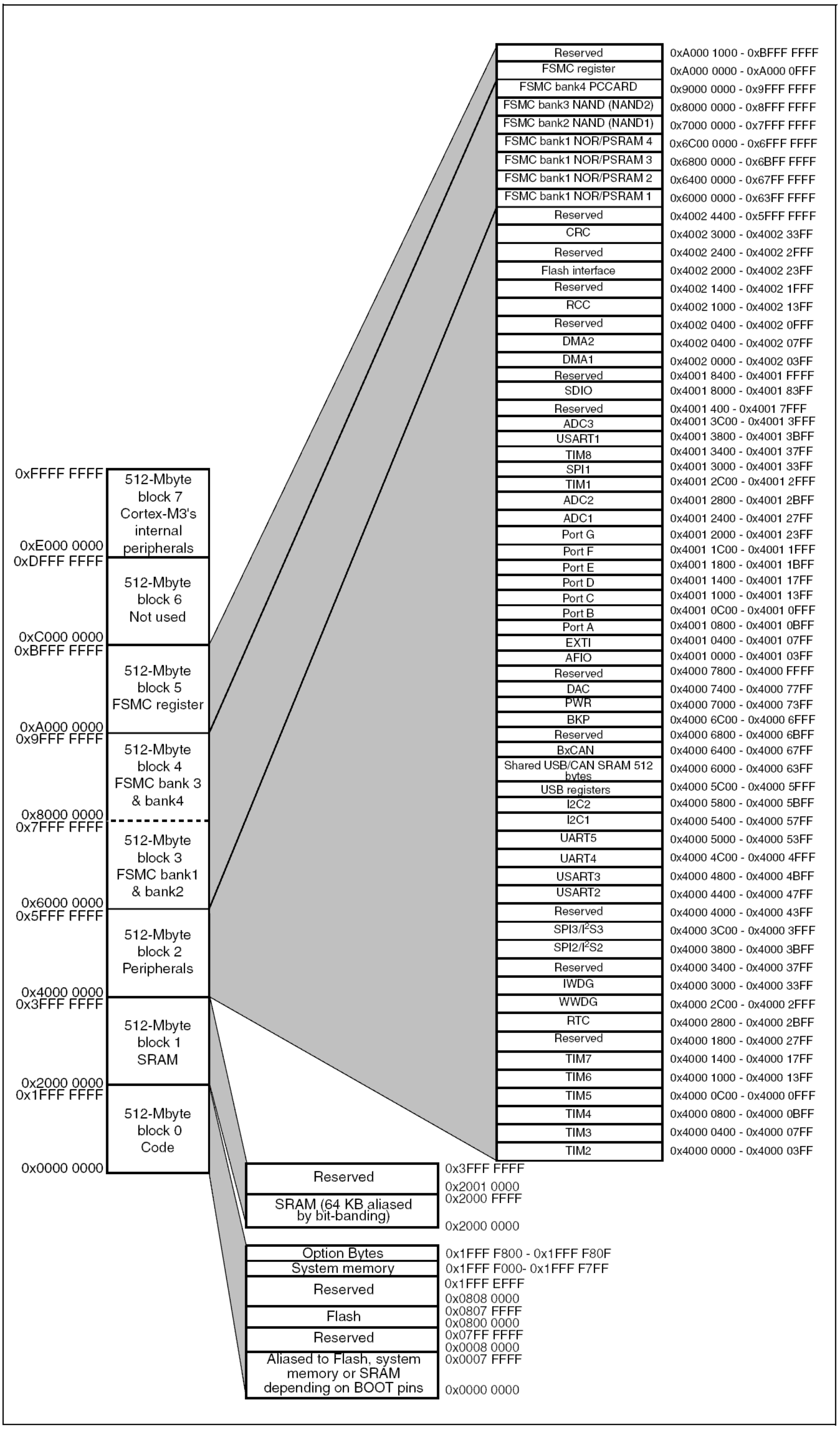
  - Sleep, Stop and Standby modes
  - VBAT supply for RTC and backup registers
- 3 × 12-bit, 1 μs A/D converters (up to 21 channels)
  - Conversion range: 0 to 3.6 V
  - Triple-sample and hold capability
  - Temperature sensor
- 2 × 12-bit D/A converters
- DMA: 12-channel DMA controller
  - Supported peripherals: timers, ADCs, DAC, SDIO, I^2Ss, SPIs, I^2Cs and USARTs
- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
  - Cortex-M3 Embedded Trace Macrocell™
- 112 fast I/O ports
  - 112 I/Os, all mappable on 16 external interrupt vectors, all 5 V-tolerant except for analog inputs
- 11 timers
  - four 16-bit timers, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - 2 × 16-bit motor control PWM timers with dead-time generation and emergency stop
  - 2 × watchdog timers (Independent and Window)
  - SysTick timer: a 24-bit downcounter
  - 2 × 16-bit basic timers to drive the DAC
- 13 communication interfaces
  - 2 × I^2C interfaces (SMBus/PMBus)
  - 5 USARTs (ISO 7816 interface, LIN, IrDA capability, modem control)
  - 3 SPIs (18 Mbit/s), 2 with I^2S interface multiplexed
  - CAN interface (2.0B Active)
  - USB 2.0 full speed interface
  - SDIO interface
- CRC calculation unit, 96-bit unique ID

BLOCK DIAGRAM:



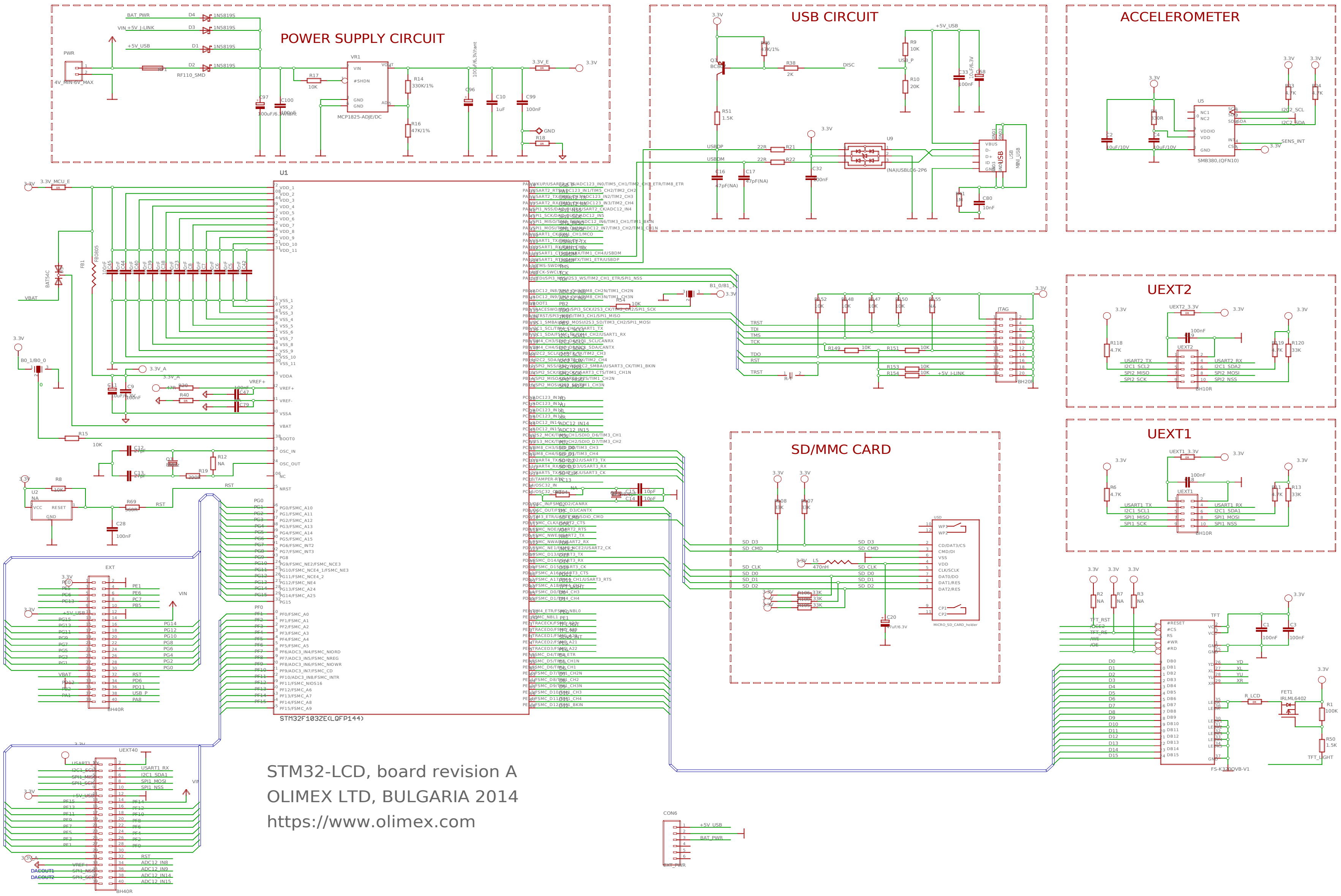
1. AF = alternate function on I/O port pin.

MEMORY MAP:

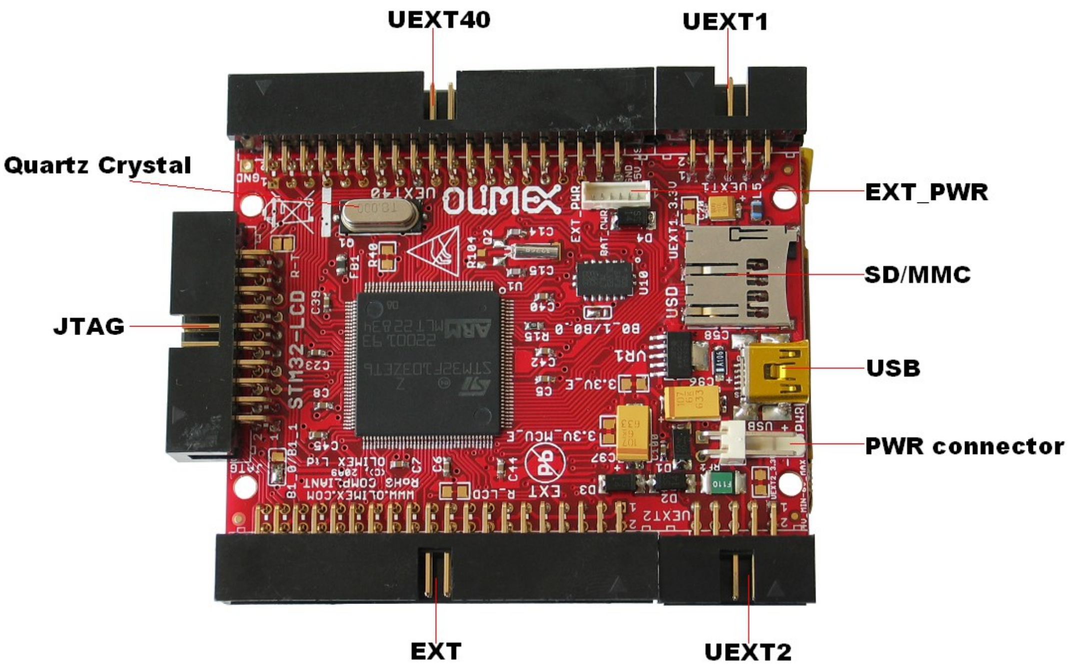


Reserved
0xA000 1000 - 0xBFFF FFFF
FSMC register
0xA000 0000 - 0xA000 0FFF
FSMC bank4 PCCARD
0x9000 0000 - 0x9FFF FFFF
FSMC bank3 NAND (NAND2)
0x8000 0000 - 0x8FFF FFFF
FSMC bank2 NAND (NAND1)
0x7000 0000 - 0x7FFF FFFF
FSMC bank1 NOR/PSRAM 4
0x6C00 0000 - 0x6FFF FFFF
FSMC bank1 NOR/PSRAM 3
0x6800 0000 - 0x6BFF FFFF
FSMC bank1 NOR/PSRAM 2
0x6400 0000 - 0x67FF FFFF
FSMC bank1 NOR/PSRAM 1
0x6000 0000 - 0x63FF FFFF
Reserved
0x4002 4400 - 0x5FFF FFFF
CRC
0x4002 3000 - 0x4002 33FF
Reserved
0x4002 2400 - 0x4002 2FFF
Flash interface
0x4002 2000 - 0x4002 23FF
Reserved
0x4002 1400 - 0x4002 1FFF
RCC
0x4002 1000 - 0x4002 13FF
Reserved
0x4002 0400 - 0x4002 0FFF
DMA2
0x4002 0400 - 0x4002 07FF
DMA1
0x4002 0000 - 0x4002 03FF
Reserved
0x4001 8400 - 0x4001 FFFF
SDIO
0x4001 8000 - 0x4001 83FF
Reserved
0x4001 400 - 0x4001 7FFF
ADC3
0x4001 3C00 - 0x4001 3FFF
USART1
0x4001 3800 - 0x4001 3BFF
TIM8
0x4001 3400 - 0x4001 37FF
SPI1
0x4001 3000 - 0x4001 33FF
TIM1
0x4001 2C00 - 0x4001 2FFF
ADC2
0x4001 2800 - 0x4001 2BFF
ADC1
0x4001 2400 - 0x4001 27FF
Port G
0x4001 2000 - 0x4001 23FF
Port F
0x4001 1C00 - 0x4001 1FFF
Port E
0x4001 1800 - 0x4001 1BFF
Port D
0x4001 1400 - 0x4001 17FF
Port C
0x4001 1000 - 0x4001 13FF
Port B
0x4001 0C00 - 0x4001 0FFF
Port A
0x4001 0800 - 0x4001 0BFF
EXTI
0x4001 0400 - 0x4001 07FF
AFIO
0x4001 0000 - 0x4001 03FF
Reserved
0x4000 7800 - 0x4000 FFFF
DAC
0x4000 7400 - 0x4000 77FF
PWR
0x4000 7000 - 0x4000 73FF
BKP
0x4000 6C00 - 0x4000 6FFF
Reserved
0x4000 6800 - 0x4000 6BFF
BxCAN
0x4000 6400 - 0x4000 67FF
Shared USB/CAN SRAM 512 bytes
0x4000 6000 - 0x4000 63FF
USB registers
0x4000 5C00 - 0x4000 5FFF
I2C2
0x4000 5800 - 0x4000 5BFF
I2C1
0x4000 5400 - 0x4000 57FF
UART5
0x4000 5000 - 0x4000 53FF
UART4
0x4000 4C00 - 0x4000 4FFF
USART3
0x4000 4800 - 0x4000 4BFF
USART2
0x4000 4400 - 0x4000 47FF
Reserved
0x4000 4000 - 0x4000 43FF
SPI3/I2S3
0x4000 3C00 - 0x4000 3FFF
SPI2/I2S2
0x4000 3800 - 0x4000 3BFF
Reserved
0x4000 3400 - 0x4000 37FF
IWDG
0x4000 3000 - 0x4000 33FF
WWDG
0x4000 2C00 - 0x4000 2FFF
RTC
0x4000 2800 - 0x4000 2BFF
Reserved
0x4000 1800 - 0x4000 27FF
TIM7
0x4000 1400 - 0x4000 17FF
TIM6
0x4000 1000 - 0x4000 13FF
TIM5
0x4000 0C00 - 0x4000 0FFF
TIM4
0x4000 0800 - 0x4000 0BFF
TIM3
0x4000 0400 - 0x4000 07FF
TIM2
0x4000 0000 - 0x4000 03FF
0xFFFF FFFF
512-Mbyte block 7 Cortex-M3's internal peripherals
0xE000 0000
0xDFFF FFFF
512-Mbyte block 6 Not used
0xC000 0000
0xBFFF FFFF
512-Mbyte block 5 FSMC register
0xA000 0000
0x9FFF FFFF
512-Mbyte block 4 FSMC bank 3 & bank4
0x8000 0000
0x7FFF FFFF
512-Mbyte block 3 FSMC bank1 & bank2
0x6000 0000
0x5FFF FFFF
512-Mbyte block 2 Peripherals
0x4000 0000
0x3FFF FFFF
512-Mbyte block 1 SRAM
0x2000 0000
0x1FFF FFFF
512-Mbyte block 0 Code
0x0000 0000
Reserved
0x3FFF FFFF
0x2001 0000
SRAM (64 KB aliased by bit-banding)
0x2000 FFFF
0x2000 0000
Option Bytes
0x1FFF F800 - 0x1FFF F80F
System memory
0x1FFF F000- 0x1FFF F7FF
Reserved
0x1FFF EFFF
0x0808 0000
Flash
0x0807 FFFF
0x0800 0000
Reserved
0x07FF FFFF
0x0008 0000
Aliased to Flash, system memory or SRAM depending on BOOT pins
0x0007 FFFF
0x0000 0000

SCHEMATIC:


POWER SUPPLY CIRCUIT
USB CIRCUIT
ACCELEROMETER
UEXT2
UEXT1
SD/MMC CARD
STM32F103ZE(LQFP144)
STM32-LCD, board revision A
OLIMEX LTD, BULGARIA 2014
https://www.olimex.com

BOARD LAYOUT



POWER SUPPLY CIRCUIT:

STM32-LCD can take power from four sources:

- Power connector – 4V – 6V DC.
- BAT_PWR from EXT_PWR – 4V DC.
- +5V_J-LINK from JTAG connector
- +5V_USB from USB connector

The programmed board power consumption is about 200 mA.

RESET CIRCUIT:

STM32-LCD reset circuit includes R8 (10k), R69 (560 Ohm), C28 (100nF) pin 15 of JTAG connector, EXT pin 32, UEXT40 pin 32 and STM32F103ZE pin 25 (NRST).

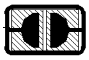
CLOCK CIRCUIT:

Quartz crystal 8 MHz is connected to STM32F103ZE pin 23 (OSC_IN) and pin 24 (OSC_OUT).

Quartz crystal 32.768 kHz is connected to STM32F103ZE pin 8 (PC14/OSC32_IN) and pin 9 (PC15/OSC32_OUT).

JUMPER DESCRIPTION:

R-T



Connect RST with TRST.
Default state is open.

UEXT1_3.3V



This jumper when closed, supplies 3.3 V voltage to UEXT1 pin 1.
Default state is closed.

UEXT2_3.3V



This jumper when closed, supplies 3.3 V voltage to UEXT2 pin 1.
Default state is closed.

3.3V_E



This jumper, when closed, enable the main 3.3 V regulator VR1 - MCP1825-ADJE/DC.
Default state is closed.

3.3V_MCU_E



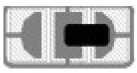
This jumper, when closed, enables STM32F103ZE 3.3 V power supply.
Default state is closed.

R_LCD



You can use this jumper, when it's open, to measure the current of LCD backlight.
Default state is closed.

B0_1/B0_0



Select BOOT0 Boot mode.
Default state is in position B0_0.

B1_0/B1_1



Select BOOT1 Boot mode.
Default state – B1_0 – not shorted and B1_1 – not shorted.

Boot mode selection pins		**Boot Mode**	**Aliasing**
BOOT1	BOOT0		
x	0	Main Flash memory	Main Flash memory is selected as boot space
0	1	System memory	System memory is selected as boot space
1	1	Embedded SRAM	Embedded SRAM is selected as boot space

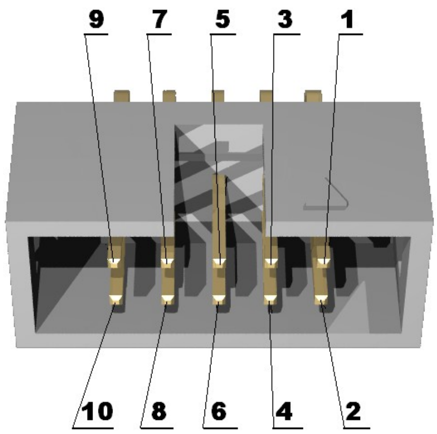
INPUT/OUTPUT:

- LCD TFT 320x240 pixels colored with touch screen.

EXTERNAL CONNECTORS DESCRIPTION:

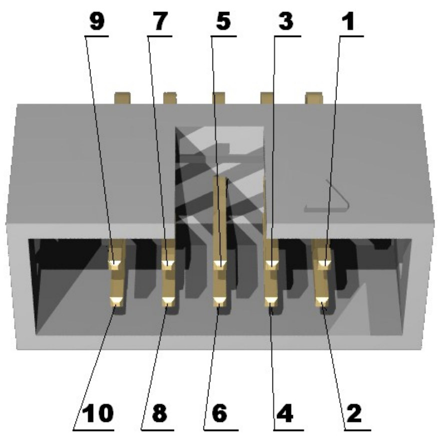
UEXT1

Pin #	Signal Name
1	3.3V
2	GND
3	USART1_TX
4	USART1_RX
5	I2C1_SCL1
6	I2C1_SDA1
7	SPI1_MISO
8	SPI1_MOSI
9	SPI1_SCK
10	SPI1_NSS

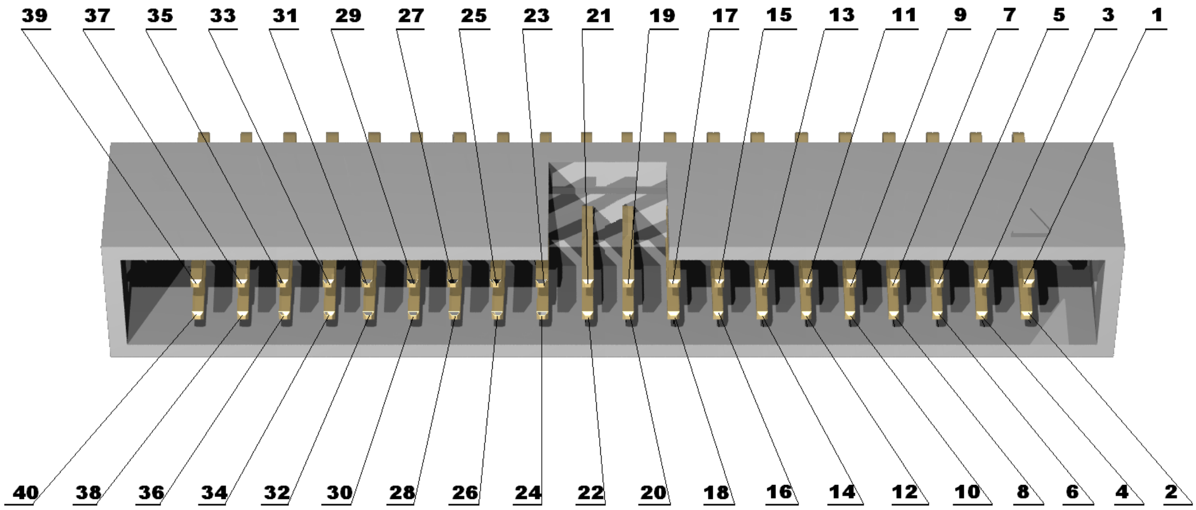


UEXT2

Pin #	Signal Name
1	3.3V
2	GND
3	USART2_TX
4	USART2_RX
5	I2C1_SCL2
6	I2C1_SDA2
7	SPI2_MISO
8	SPI2_MOSI
9	SPI2_SCK
10	SPI2_NSS

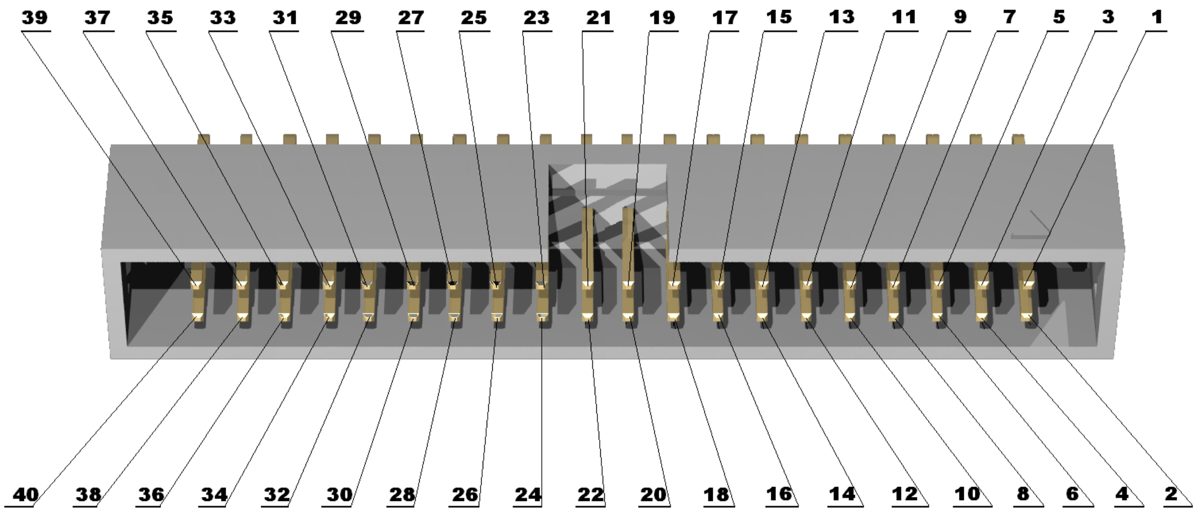


EXT



Pin #	Signal Name	Pin #	Signal Name
1	3.3 V	2	GND
3	PE0	4	PE1
5	PE5	6	PE6
7	PC6	8	PC7
9	PC13	10	PB5
11	3.3 V	12	GND
13	+5V_USB	14	VIN
15	PG15	16	PG14
17	PG13	18	PG12
19	PG11	20	PG10
21	PG9	22	PG8
23	PG7	24	PG6
25	PG5	26	PG4
27	PG3	28	PG2
29	PG1	30	PG0
31	VBAT	32	RST
33	GND	34	PD6
35	PD12	36	PD11
37	PB2	38	USB_P
39	PA1	40	PA8

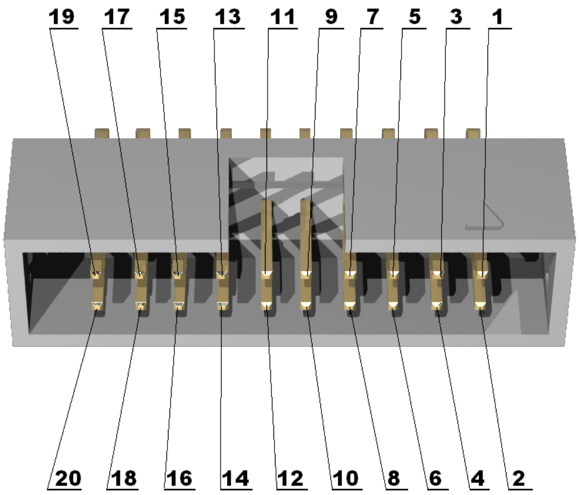
UEXT40



Pin #	Signal Name	Pin #	Signal Name
1	3.3 V	2	GND
3	USART1_TX	4	USART1_RX
5	I2C1_SCL1	6	I2C1_SDA1
7	SPI1_MISO	8	SPI1_MOSI
9	SPI1_SCK	10	SPI1_NSS
11	3.3 V	12	GND
13	+5V_USB	14	VIN
15	PF15	16	PF14
17	PF13	18	PF12
19	PF11	20	PF10
21	PF9	22	PF8
23	PF7	24	PF6
25	PF5	26	PF4
27	PF3	28	PF2
29	PF1	30	PF0
31	3.3V_A	32	RST
33	AGND	34	ADC12_IN8
35	VREF+	36	ADC12_IN9
37	SPI1_NSS	38	ADC12_IN14
39	SPI1_SCK	40	ADC12_IN15

JTAG:

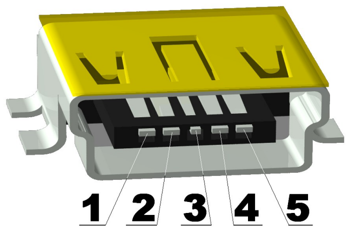
The JTAG connector allows a debugger or programmer to talk via a JTAG (Joint Test Action Group) port directly to the core. Instructions may be inserted and executed by the core thus allowing STM32F103ZE memory to be programmed with code and executed step by step by the host software.



Pin #	Signal Name	Pin #	Signal Name
1	3.3V	2	3.3V
3	TRST	4	GND
5	TDI	6	GND
7	TMS	8	GND
9	TCK	10	GND
11	pull-down	12	GND
13	TDO	14	GND
15	RST	16	GND
17	pull-down	18	GND
19	+5V J-LINK	20	GND

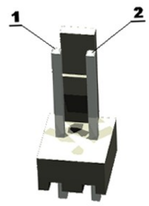
USB

Pin #	Signal Name
1	+5V_USB
2	USBDM
3	USBDP
4	NC
5	GND



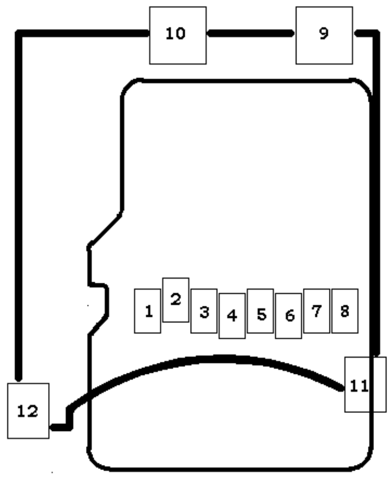
PWR

Pin #	Signal Name
1	VIN (4 – 6) V DC
2	GND



SD/MMC

Pin #	Signal Name
1	SD_D2
2	SD_D3
3	SD_CMD
4	VDD (3.3V)
5	SD_CLK
6	GND
7	SD_D0
8	SD_D1
9	Not connected
10	Not connected
11	Not connected
12	Not connected



SPI

Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

All SPIs can be served by the DMA controller.

I^2S

Two standard I^2S interfaces (multiplexed with SPI2 and SPI3) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 48 kHz are supported. When either or both of the I2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

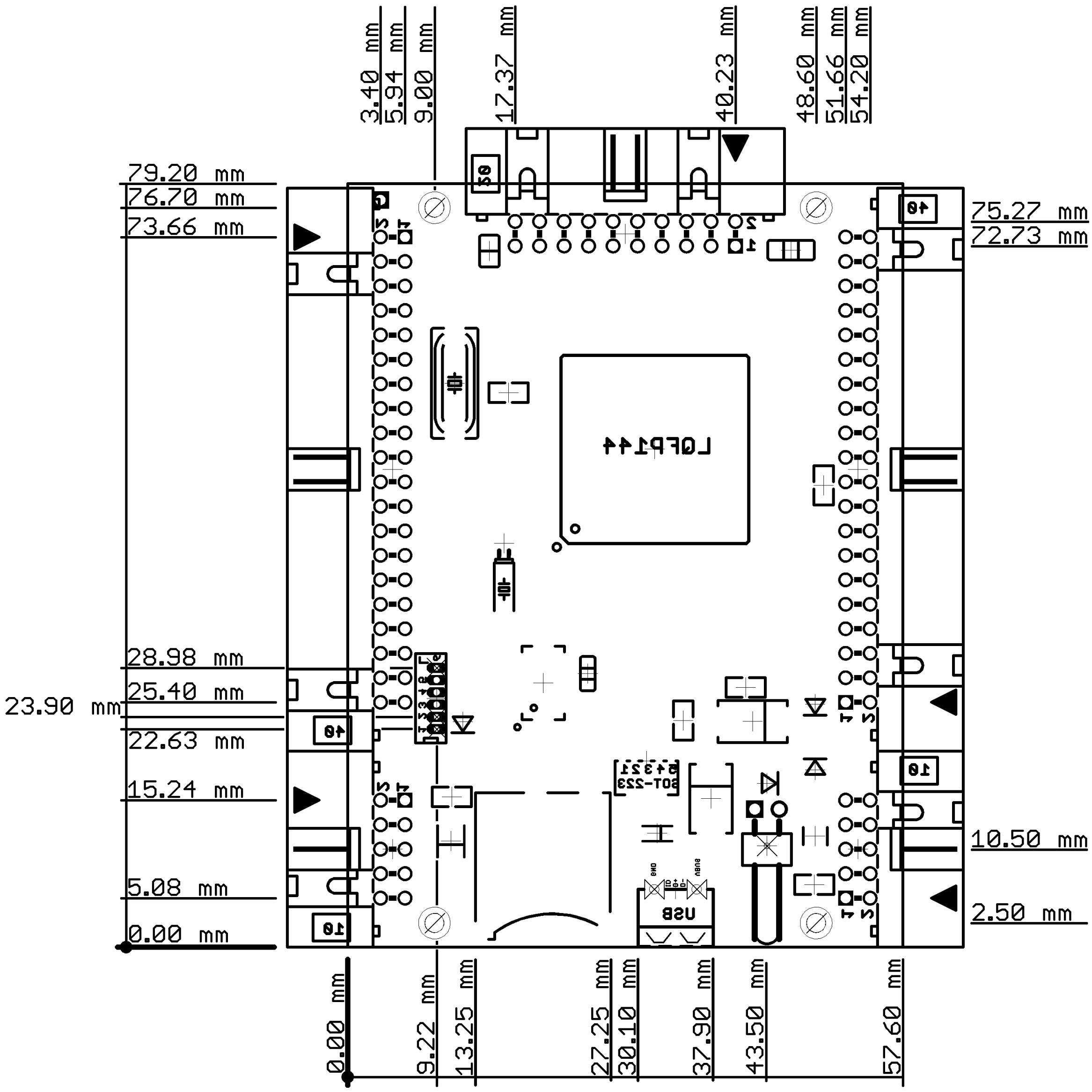
I^2C

Up to two I^2C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

MECHANICAL DIMENSIONS



AVAILABLE DEMO SOFTWARE

– EW-ARM general demo code – the code of the initial STM32-LCD demo
– EW-ARM Demo code for MOD-GSM and MOD-GSM-EDGE - (high speed) GSM modules connected to STM32-LCD

ORDER CODE: **STM32-LCD** – assembled and tested board

How to order?

You can order directly from us or from any of our distributors.
Please check our web-site https://www.olimex.com for more info.

Revision history:

Manual revision:	Rev. Initial, May 2009
	Rev. A, June 2011 – changed schematic
	Rev. B, October 2011 – added more detailed mechanical dimensions
	Rev. C, May 2014 – updated board schematic, added board revision history, updated disclaimer, updated links
Board revision:	Rev. Initial, May 2009
	Rev. A, May 2014
	1. The analog GND got properly connected to the digital GND through a 0 Ohm resistor
	2. Fixed the JTAG label (was "JATG" before)
	3. The LCD GND got properly connected
	4. The cathodes of the LCD 's backlight got connected to GND
	5. C1 i C3 are moved further away from the LCD connector
	6. The accelerometer is changed from LISxx to SMB380
	7. Added RC filter to the power suppl of SMB380

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It is possible that the pictures in this manual differ from the latest revision of the board.

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THERE IS NO WARRANTY FOR THE DESIGN MATERIALS AND THE COMPONENTS USED TO CREATE STM32-LCD. THEY ARE CONSIDERED SUITABLE ONLY FOR STM32-LCD.